

LUCUS MAXIMUS KIM

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EDUCATION

Texas A&M University – College Station, TX

B.S. Computer Engineering, Brown Engineering Honors — May 2027

M.S. Computer Engineering (Fast Track) — Expected **Fall 2028**

Cumulative GPA: 3.71 / 4.0

Minor in Mathematics

TECHNICAL SKILLS

- **HDL & Verification:** Verilog, VHDL, SystemC, RTL design, testbench development, functional simulation, waveform debug (GTKWave, Icarus Verilog, Vivado)
- **Timing & Physical Design:** Static Timing Analysis (STA), timing closure, setup/hold, slack, critical path analysis, retiming, clock domains, clock gating, latch-based design, Vt/drive-strength optimization, DFT/scan awareness
- **Computer Architecture:** pipelining, hazard detection & forwarding, branch prediction, out-of-order execution, cache hierarchy, cache coherence (MESI/MOESI), memory hierarchy, ZSim, ChampSim, SPEC CPU2006, PARSEC
- **Languages & Tools:** Python, C++, C, Java, Bash, Git, Linux/UNIX, Make, NumPy, LTspice, Arduino, Raspberry Pi

EXPERIENCE

Hardware Developer Intern — IBM, Z Logic Processor — Austin, TX

May 2026 – August 2026

- Performed static timing analysis (STA) on a next-generation IBM Z processor unit, triaging failing setup paths across the macro/unit hierarchy and recovering negative slack via latch extraction, gate moves (retiming across cycle boundaries), latch cloning, and Vt/drive-strength type upgrades.
- Built "Slack Zero," an agentic AI timing-closure assistant (Python, MCP tooling) that parses timing-report exports, classifies 900+ failing paths into ranked fix categories, and validates each recommendation against live path-trace queries, reducing manual triage from 2 weeks to 10 minutes.
- Encoded the team's timing-closure methodology as a deterministic decision tree with structural safety checks, fanout/broadcast-latch detection, adjacent-cycle headroom analysis, clock-domain and clock-gating (LCB) cost modeling, shared-net verification, emitting per-path confidence and audit-traceable verdicts.

Undergraduate Research Assistant — Texas A&M University

August 2025 – May 2026

- Extended a RocksDB key-value store with content-based semantic retrieval, integrating text embeddings as an indexing mechanism to return files by similarity rather than exact-key lookup. Condensed multi-vector ColBERT retrieval outputs into fixed-dimension encodings (FDEs) via Google's MUVERA algorithm; tuned parameterization on the QUORA dataset.

PERSONAL PROJECTS

Mockingjay LLC Cache Replacement Policy in ZSim — C++

February 2026 – May 2026

- Ported the Mockingjay replacement policy (multi-class PC-based reuse-distance prediction, HPCA '22) from ChampSim to the ZSim execution-driven simulator; modified the memory hierarchy to propagate program-counter signatures from L1/L2 to the last-level cache (LLC) and implemented a cache-bypass mechanism.
- Implemented the sampled cache, reuse distance predictor (hashed PC signature, 7-bit saturating counters), and 5-bit ETR counters; evaluated against LRU/LFU/SRRIP across SPEC CPU2006 and 8-core PARSEC (500M / 5B instruction)
- Achieved 18.4% IPC speedup on mcf and 58.7% on streamcluster over LRU with large MPKI reductions; root-caused multicore regressions to MESI coherence incompatibility with line bypass and infinite-ETR initialization on PCs.

RISC-V 5-Stage Pipelined CPU Core — Verilog

May 2025 – June 2025

- Implemented a 5-stage pipelined RV32I RISC-V CPU core in Verilog, featuring instruction fetch, decode, execute, memory, and write-back stages. Verified design entirely in simulation using Icarus Verilog and GTKWave.
- Wrote comprehensive test-benches and achieved full instruction set compliance across 30+ simulated programs. Debugged pipeline hazards, forwarding, and branch prediction behavior with waveform analysis tools.

Single-Cycle ARMv8 Processor Implementation — Verilog

February 2025 – May 2025

- Constructed a complete single-cycle ARMv8 processor in Verilog, integrating both control and datapath modules. Connected core components: ALU, data & instruction memory, register file, multiplexers, sign extender, etc.

LEADERSHIP EXPERIENCE

Beta Tau Omega Fraternity Inc.

May 2024 – Present

Parliamentarian

- Ideated a digital attendance tracking system to monitor task completion and event participation across 50+ members, automated reporting with Python. Automated reporting via a companion iOS app.
- Administered 8 community service outings as Philanthropy Chair, assembling 80% of fraternity members to support the Adopt-A-Street program and strengthen campus-community relations.